UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,519	09/24/2001	Koutarou Tagawa	1448.1015	7245

21171 7590 12/15/2004

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,519	TAGAWA ET AL.	
	Examiner	Art Unit	
	Michael C Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,10 and 11* is/are rejected.

7)☒ Claim(s) *2-4,7-9 and 12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Office Action

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 5, 6, and 10, are rejected under 35 U.S.C. 102(e) as being anticipated by Nagatome, U.S. Patent 6,339,753 B1.

Referring to claim 1:

a. In column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU and an in-circuit emulator (a microcomputer with a debug supporting function in which a program to be executed by a CPU is debugged using an in-circuit emulator).

b. In column 3, lines 62-66, Nagatome discloses that the simulator chip includes a CPU block and a peripheral block. A first power supply is connected to the designation unit and the CPU block, while a second power supply is connected to the peripheral block and the microcomputer application system (a debug target circuit having the CPU as a component and in which supply and stop of drive power can be arbitrarily switched).

c. In column 3, lines 57-61, Nagatome discloses that the in-circuit emulator includes a simulator chip that simulates the operation of the microcomputer. The in-circuit emulator further includes a designation unit, which is realized with a RAM or the like, simulating a read only memory (ROM) in the microcomputer application system. The designation unit is designed to supply instruction signals to the simulator chip (a debugging circuit which has an interface module to the in-circuit emulator and which holds a debug related setting by drive power supplied thereto, independently of the debug target circuit). Further, in column 3, lines 62-66, Nagatome discloses a first power supply is connected to the designation unit and the CPU block (holds a debug related setting by drive power supplied in a condition in which drive power to the debug target circuit is stopped).

Referring to claims 5 and 10 in column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU (wherein the microcomputer is a microcontroller or a microprocessor).

Referring to claim 6:

a. In column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU and an in-circuit emulator (a microcomputer with a debug supporting function in which a program to be executed by a CPU is debugged using an in-circuit emulator).

b. In column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU (a debug target circuit having the CPU as a component).

c. In column 3, lines 57-61, Nagatome discloses that the in-circuit emulator includes a simulator chip that simulates the operation of the microcomputer. The in-circuit emulator further includes a designation unit, which is realized with a RAM or the like, simulating a read only memory (ROM) in the microcomputer application system. The designation unit is designed to supply instruction signals to the simulator chip (a debugging circuit which has an interface module to the in-circuit emulator).

d. In column 3, lines 62-66, Nagatome discloses that a second power supply is connected to the peripheral block and the microcomputer application system (a first power supply terminal which supplies an external drive power to the debug target circuit).

e. In column 3, lines 62-66, Nagatome discloses that the simulator chip includes a CPU block and a peripheral block. A first power supply is connected to the designation unit and the CPU block (a second power supply terminal which supplies an external drive power to the debugging circuit independently of power supply to the debug target circuit).

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 11 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Nagatome U.S. Patent 6,339,753 B1.

Referring to claim 11:

a. In column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU and an in-circuit emulator (a microcomputer with a debug supporting function in which a program to be executed by a CPU is debugged using an in-circuit emulator).

b. In column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU (a debug target circuit having the CPU as a component).

c. In column 3, lines 57-61, Nagatome discloses that the in-circuit emulator includes a simulator chip that simulates the operation of the microcomputer. The in-circuit emulator further includes a designation unit, which is realized with a RAM or the like, simulating a read only memory (ROM) in the microcomputer application system. The designation unit is designed to supply instruction signals to the simulator chip (a debugging circuit which has an interface module to the in-circuit emulator).

d. In column 3, lines 62-66, Nagatome discloses that a second power supply is connected to the peripheral block and the microcomputer application system (a

first power supply terminal which supplies an external drive power to the debug target circuit).

e. In column 3, lines 62-66, Nagatome discloses a power supply. However, Nagatome doesn't explicitly disclose a switching element which switches supply and stop of the external drive power supplied through the power supply terminal to the debug target circuit; and a switch control terminal to which a control signal for controlling the switching of the switching element is supplied from outside. The Examiner takes Official Notice that a switch for controlling the power supply of a CPU is well known. An example of this is the power switch/button located on the outside of the case for the computer. It would have been obvious to one of ordinary skill at the time of the invention to include a power switch into the system of Nagatome. A person of ordinary skill in the art would have been motivated to make the modification because a switch gives the user the ability to switch the power on and off without having to unplug the power supply from an electrical outlet or battery. The design is simplified and more convenient to a user.

Referring to claim 15 in column 3, lines 55-61, Nagatome discloses a microcomputer application system including a CPU (wherein the microcomputer is a microcontroller or a microprocessor).

Allowable Subject Matter

6. Claims 2, 3, 4, 7, 8, 9, 12, 13, and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed December 2, 2004 have been fully considered but they are not persuasive.

8. On page 6, under the section NAGATOME U.S. PATENT 6,339,753 DISCLOSES NO MORE THAN THE ADMITTED PRIOR ART OF FIG. 1, the Applicant argues, "Nagatome merely discloses, in Fig. 2, that designation unit 42, which corresponds to the debugging circuit in the present invention, and simulator chip 41, which corresponds to the debug target circuit in the present invention and simulates operation of microcomputer 21 controlled by the designation unit 42, both disposed within ICE 40, are driven by the same power source, namely power supply 43a. Nagatome thus discloses what applicants regard as the conventional art for the present invention, as shown in Fig. 1 of the present application. Therefore, Nagatome, being no different from the admitted prior of Fig. 1 of the present application, cannot stop the supply of driving power to the simulator chip 41 when the designation unit 42 is in operation, being driven by the driving power supplied thereto. Therefore, the present invention is neither anticipated by nor obvious in view of the cited reference." The Examiner respectfully disagrees. The figure that the Applicant directs the Examiner to in the present Application doesn't show a power supply at all. It is unclear as to where

the differences lie when the figure relied upon by the Applicant fails to show anything that resembles the device in the Nagatome reference. The Examiner directs the Applicant to Figure 2 of Nagatome, which clearly shows **two** power supplies much like the Applicant's claimed invention. Further, the Applicant has mistakenly corresponded the simulator chip 41, of Nagatome with the debug target circuit of the claimed invention. The debug target circuit of the Applicant's claimed invention corresponds to the reference number 20 of Figure 2, which is shown as being supplied separately and independently by its own power supply. To expedite prosecution the Examiner suggests incorporating the allowable subject matter of claims 2, 3, 4, 7, 8, 9, 12, 13, and 14 into the independent claims.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2